IMPLEMENTATION AND PERFORMANCE OF A HIGH-SPEED, VHDL-BASED, MULTI-MODE ARTM DEMODULATOR

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ABSTRACT

Legacy telemetry systems, although widely deployed, are being severely taxed to support the high data rate requirements of advanced aircraft and missile platforms. Increasing data rates, in conjunction with loss of spectrum have created a need to use available spectrum more efficiently. In response to this, new modulation techniques have been developed which offer more data capacity in the same operating bandwidth. Demodulation of these new waveforms is a computationally challenging task, especially at high data rates. This paper describes the design, implementation and performance of a high-speed, multi-mode demodulator for the Advanced Range Telemetry (ARTM) program which meets these challenges.

KEY WORDS

FPGA, VHDL, Software Defined Radio, Reconfigurable Hardware

INTRODUCTION

For many years pulse code modulation / frequency modulation (PCM/FM) has been ubiquitous in the telemetry community. While offering the advantages of low cost, simple implementation, and excellent interoperability between equipments offered by different vendors, it has the increasingly serious disadvantage of requiring a relatively large operating bandwidth. In the mid-90's, the Advanced Range Telemetry (ARTM) program was initiated to find ways of making better use of the available spectrum. Out of this program first emerged the Tier I modulation techniques (FQPSK-B Rev A1, and SOQPSK) and later the Tier II waveform (multi-h CPM). Furthermore, the research which produced the advanced demodulators for these waveforms also resulted in a breakthrough in demodulation of PCM/FM, resulting in a 3 dB improvement in detection efficiency with no changes to installed transmitters. This paper will describe a

demodulator which is software configurable to demodulate both the Tier I and Tier II ARTM waveforms, or improve the detection efficiency of the legacy PCM/FM signals.

THE WAVEFORMS

Several excellent papers have been published describing the ARTM waveforms, so we will only briefly describe them here. For the sake of simplicity, we will refer to the legacy PCM/FM waveform as ARTM Tier 0, even though this technique has been in use since long before the ARTM program was launched. (The enhanced demodulator for this waveform, however, was developed under the ARTM program, so it's not unreasonable to call it the ARTM Tier 0 demodulator.) When we refer to Tier I waveforms, we will mean either FQSPK-B or SOQPSK, as these modulations are interoperable, and essentially indistinguishable. The Tier II waveform refers to the particular variant of multi-h continuous phase modulation (CPM) which has been implemented under the ARTM program.

Table 1 summarizes the key features of these three waveforms, and their time domain and frequency domain characteristics are depicted in Figure 1.

	PCM/FM (Tier 0)	SOQPSK (Tier 1)	Multi-h CPM (Tier 2)
Bandwidth Efficiency relative to PCM/FM	1x	2x	3x
Link Margin relative to conventional PCM/FM	3 dB	0 dB	0 dB
Compatibility	Existing transmitters	Compatible with FQPSK	Ideal for new designs

Table 1. Key features of PCM/FM, SOQPSK, and Multi-h CPM.

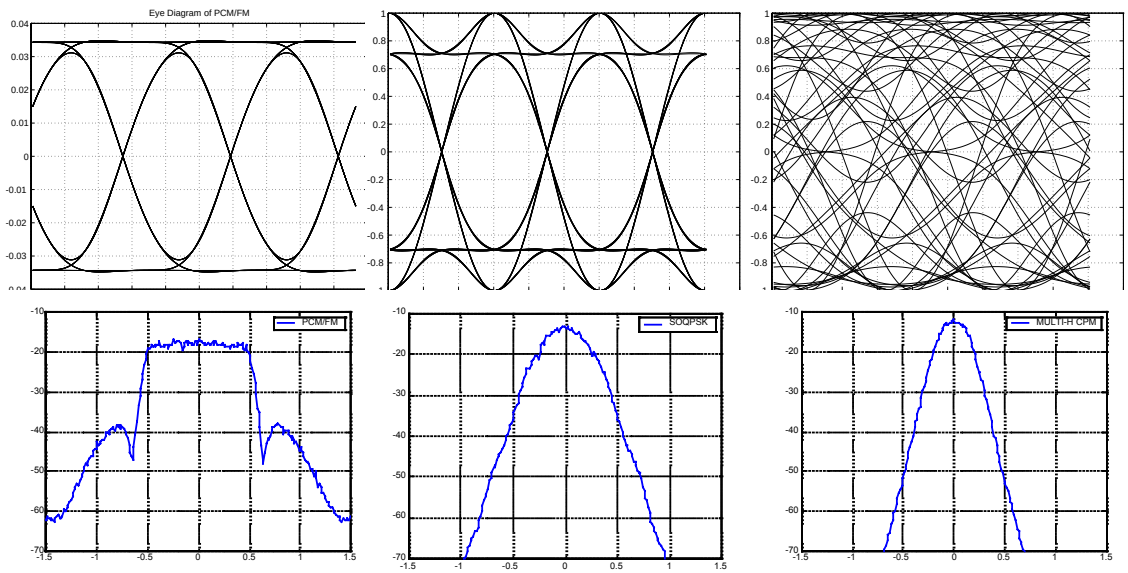

Figure 1. Time- and frequency-domain characteristics of PCM/FM (left), SOQPSK (center), and Multi-h CPM (right).

THE DEMODULATOR

A photo of the MMD22 (multi-mode demodulator, 22 Mbps) Hypermod demodulator appears in Figure 2, and Figure 3 below depicts a top-level block diagram of the Demodulator; at this level, there is no distinction between the three operating modes. Figures 4, 5, and 6, however, show how the signal flows are radically modified for each of the three different modulations. It is only through the reprogrammability of the hardware that such completely different signal processing paths can be constructed in a single piece of hardware.

The key feature of the MMD22 which supports its multi-mode operation is that virtually of the signal processing is performed in a set of five interconnected Xilinx VirtexE 2000 field programmable gate arrays (FPGA), comprising over 12.5 million gates. Some other salient features of this set of devices are summarized in Table 2.

System gates	12.5 Million
Logic gates	2,592,000
Logic cells	216,000
Dedicated Block RAM	3,276,800
Logic Cell RAM	3,072,000
I/O pins	2020

Table 2. MMD22 signal processing engine characteristics.

Figure 2. MMD22 Demodulator

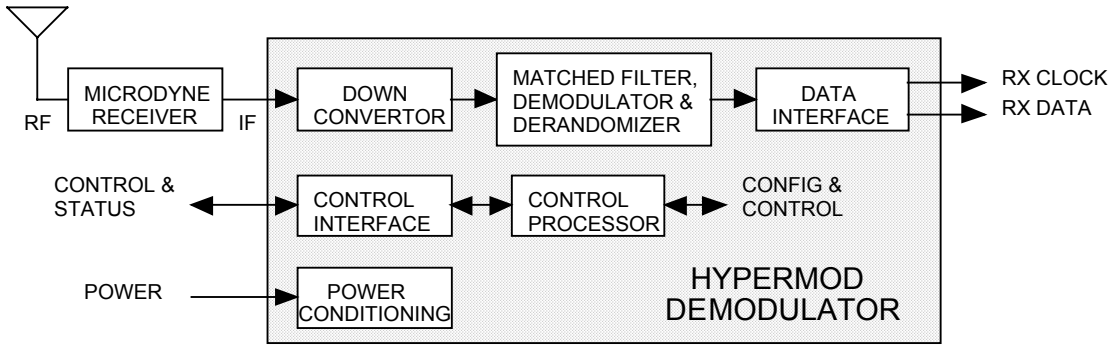

Figure 3. Overview of MMD22 Demodulator.

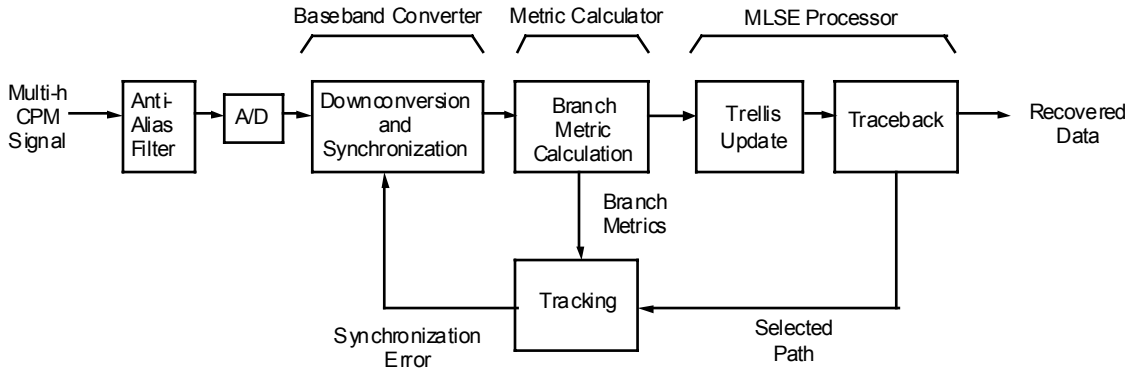

Figure 4. Multi-h CPM (Tier 2) Configuration.

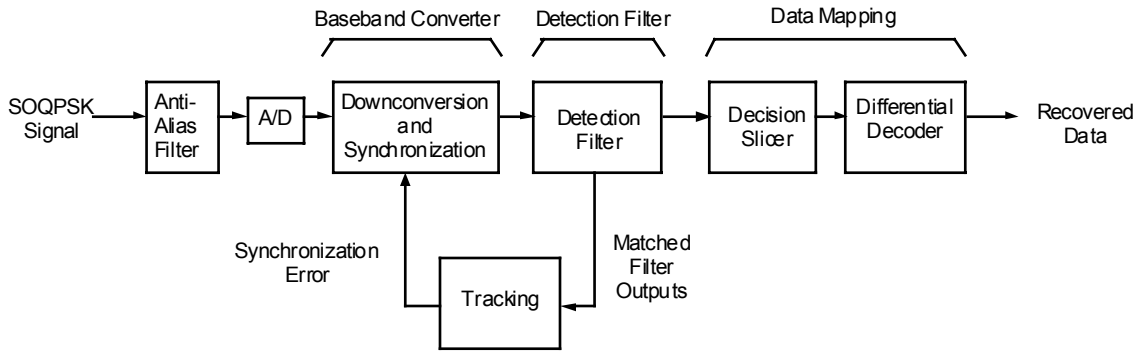

Figure 5. SOQPSK (Tier 1) Configuration..

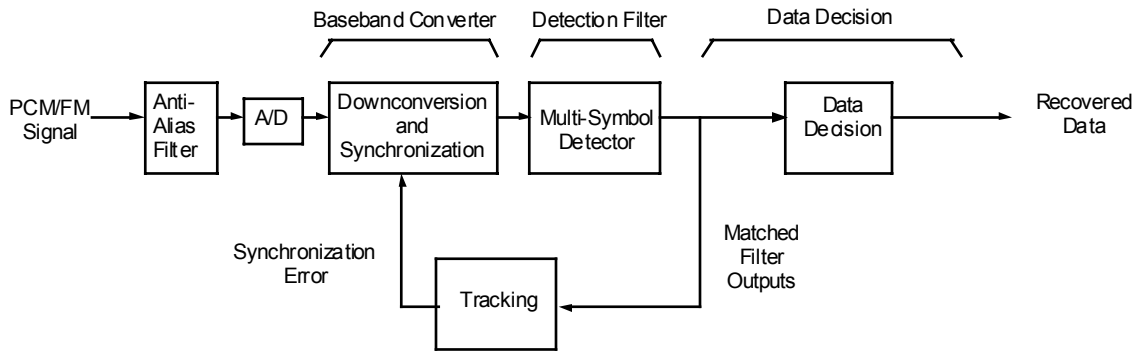

Figure 6. PCM/FM (Tier 0) Configuration

In the Multi-h CPM (Tier 2) configuration shown in Figure 4, the MMD22 signal processing path includes five separate functions, final downconversion and synchronization (which includes resampling and digital IF filtering), branch metric calculation, trellis decoder, traceback, and tracking. For this waveform, the trellis is 128 states wide, fed by 512 complex-valued branch metrics. Each branch metric feeds 8 states of the trellis. The routing pattern this creates is not symmetrical and consumes large amounts of routing resources. The trellis decoder alone used 80% of the logic, 40% of the block RAM, and 95% of the I/O pins of a Xilinx XVC2000E. The XVC2000E was the only FPGA on the market which had sufficient speed, I/O, logic elements, block memory and routing resources to make the CPM trellis decoder possible in a single FPGA. The same device was used for the other four FPGAs to provide for future product features, such as adaptive equalization to combat multipath.

The trellis connections for the CPM waveform are extremely complex, so a Matlab simulation of the trellis decoder was used to actually write the VHDL which loads the FPGAs. The Matlab model had all of the trellis connections built in to it, making it practical to use it to write the VHDL file as an output. This saved countless hours of time it would have taken to edit and update a VHDL source file for the trellis decoder.

Depicted in Figure 5 is the signal processing path for the Tier 1 waveform (SOQPSK). (Thorough testing has shown that this configuration of the demodulator performs almost

identically with the other Tier 1 waveform, Feher-patented FQPSK-B, Revision A1.) In this configuration, the demodulation process is quite conventional, although the digital detection filtering offers an improvement in detection efficiency by allowing the synthesis of a matched filter which is better suited to the Tier 1 waveform.

Figure 6 shows the hardware configuration for PCM/FM (Tier 0). While PCM/FM has a long history in the telemetry community, and is used on virtually all telemetry missions flying today, the MMD22 offers a truly significant enhancement to the demodulation of this waveform.

Instead of a conventional single-symbol detection technique, the PCM/FM demodulator in the MMD22 uses a multiple symbol detection algorithm, as depicted in Figure 7. Like both the Tier 2 and Tier 1 modulations, the Tier 0 waveform can be defined by a phase trellis. In effect, knowledge of the previous symbols, which define the path through the trellis, can be used to make more reliable decisions about the present symbol. Looking at future symbols (by delaying the decision on the present symbol) can likewise help estimate the present symbol. The MMD22 exploits this information to provide detection efficiency which is more than 3 dB better than that achieved with a single-symbol method.

Figure 8 is a photograph of the signal processing board in the MMD22. The five large devices are the FPGAs, which are reconfigured to support the three different modulation techniques.

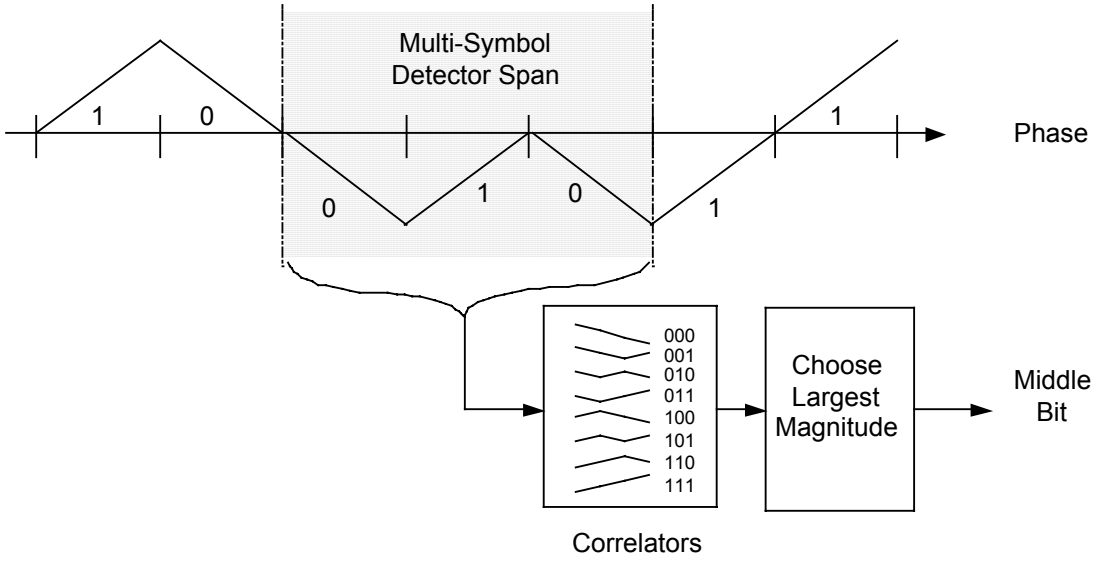

Figure 7. Multi-symbol Detection Approach for PCM/FM.

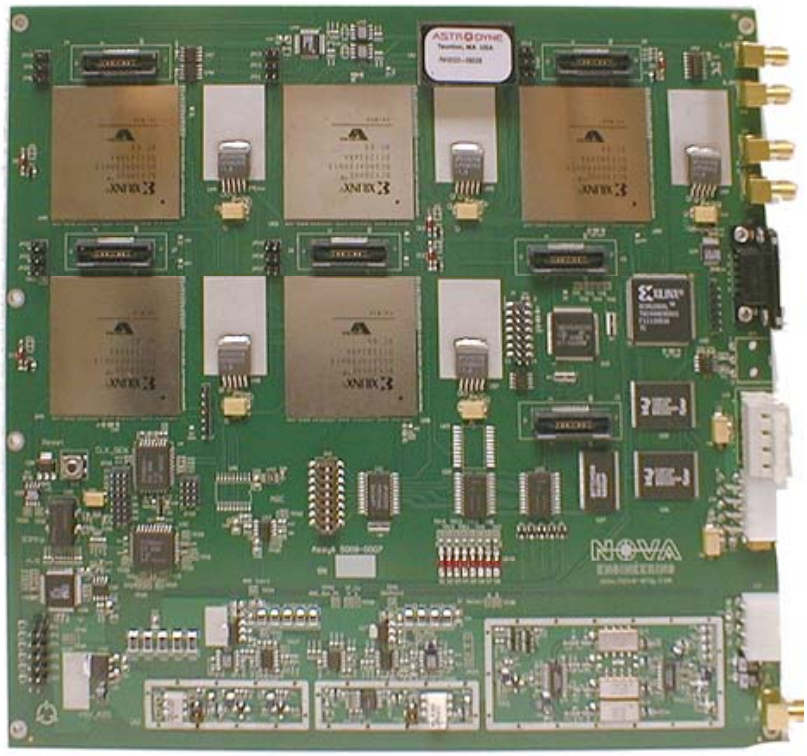

Figure 8. Signal Processing Board in the MMD22.

PERFORMANCE

The measured bit error rate performance of the MMD22 is shown in Figure 9, along with the performance of a state of the art conventional PCM/FM demodulator. The red curve, without markers, represents the performance of PCM/FM, using conventional single-symbol demodulation. This is the operating baseline of virtually every telemetry link operating today. The left-most curve is the performance of the same Tier 0 transmitters, but using the multi-symbol demodulator of the MMD22, providing a 3 dB improvement. The other two curves, for the Tier 1 and Tier 2 waveforms, quantify the performance of links with double and triple the data capacity, respectively, in the same bandwidth.

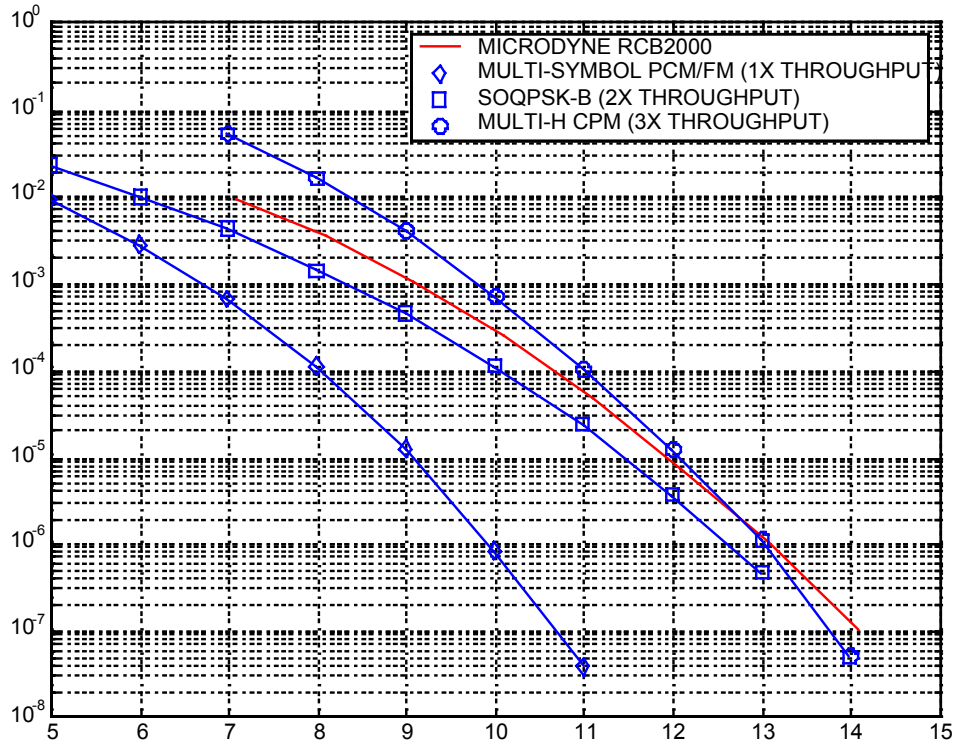

Figure 9. Bit Error Rate Performance of the MMD22.

FUTURE DEVELOPMENTS

The reprogrammability of the MMD22 has facilitated the continuing evolution of the signal processing algorithms in each of the three modes. Changes to filter characteristics, tracking loop bandwidths, threshold settings, synchronization approaches, etc. are all accomplished on a time scale measured in hours, not weeks or months. This flexibility allows lessons learned in both lab and field testing to be leveraged into design improvements, even after units are operating in the field. Nevertheless, there is room for even greater improvement, which is now underway.

The VirtexE 2000 devices used in the MMD22 were the largest, fastest FPGAs available at the start of the development. Since that time, the Virtex2 family of FPGAs has been introduced, and the MMD44, based on the Virtex2, is presently under development. This upgrade improves the design in a number of areas. For instance, the MMD22 uses numerous multipliers that are implemented in slice logic. The Virtex2 family frees up all the multiplier logic by making use of the wide hardware multipliers on the silicon. These multipliers are 3X to 4X faster and use only 2 piping stages instead of the 4 or 5 needed for the first generation design. This translates into less latency in the tracking loops, and better performance. The overall device speed increase with the Virtex2 parts will support much higher data rates (up to 44 Mbps). In addition, the additional computational capacity of these devices allows for higher precision arithmetic, which translates to better bit error rates. Perhaps most importantly, the Virtex2 devices provide far more logic cells, which will be used to implement new features such as adaptive equalization, to correct multi-path distortion, and forward error correction, to improve detection efficiency.

CONCLUSIONS

The advent of large, fast FPGAs has opened the door to the implementation of complex signal processing algorithms which have previously been largely theoretical abstractions. The multi-mode demodulator described here uses over twelve million gates of reconfigurable logic to implement not only one, but three, such processing techniques. To enhance the performance of existing (Tier 0) telemetry links, the multi-symbol demodulator offers a 3 dB improvement in detection efficiency. In the same package, by only reloading the FPGAs, a Tier 1 demodulator compatible with both SOQPSK and Feher-patented FQPSK-B Revision A1 offers double the data capacity in the same bandwidth. For even higher spectral efficiency, the third mode of operation performs trellis demodulation of multi-h CPM, offering triple the data capacity of PCM/FM in the same bandwidth.

Ongoing upgrades and a migration to even larger and faster FPGAs holds the promise of even further enhancement of the design.

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REFERENCES

1. T. Hill, “An Enhanced, Constant Envelope, Interoperable Shaped Offset QPSK (SOQPSK) Waveform for Improved Spectral Efficiency”, Proceedings of the International Telemetering Conference, San Diego, CA, October 2000.
2. M. Geoghegan, “ Implementation and Performance Results for Trellis Detection of SOQPSK”, Proceedings of the International Telemetering Conference, Las Vegas, NV, October 2001.
3. J.B. Anderson, T. Aulin, C.E. Sunberg, Digital Phase Modulation, Plenum Press, New York NY, 1986
4. I. Sasase, S. Mori, "Multi-h Phase Coded Modulation", IEEE Communications Magazine, Vol. 29, No. 12, December 1991
5. E.Law, K.Feher, "FQPSK Versus PCM/FM for Aeronautical Telemetry Applications; Spectral Occupancy and Bit Error Probability Comparisons", Proceedings of the International Telemetering Conference, Las Vegas, October 27-30, 1997
6. A. Premji, D.P. Taylor, "A Practical Receiver Structure for Multi-h CPM Signals", IEEE Trans. On Communications, Vol. Com-35, No. 9, September 1987
7. J.G. Proakis, Digital Communications, McGraw Hill Book Company, 1995