SOQPSK WITH LDPC:
SPENDING BANDWIDTH TO BUY LINK MARGIN

Terry Hill, Jim Uetrecht
Quasonix, West Chester, OH

Abstract: Over the past decade, SOQPSK has been widely adopted by the flight test community, and the low density parity check (LDPC) codes are now in widespread use in many applictions. This paper defines the waveform and presents the bit error rate (BER) performance of SOQPSK coupled with a rate 2/3 LDPC code. The scheme described here expands the transmission bandwidth by approximately 56% (which is still 22% less than the legacy PCM/FM modulation), for the benefit of improving link margin by over 10 dB at BER = 10^{-6}.

Keywords: SOQPSK, Shaped Offset QPSK, LDPC, ARTM Tier I, Forward Error Correction

1. INTRODUCTION

Introduced in 2000 [1], Shaped Offset QPSK (SOQPSK) occupies half the bandwidth of the legacy PCM/FM modulation, with little or no penalty in detection efficiency. After its incorporation into IRIG-106 in 2004, the adoption of SOQPSK began to accelerate. The majority of the telemetry transmitters and receivers delivered in the past few years have included SOQPSK capability. In fact, most new flight test programs are using SOQPSK as the baseline modulation, because of its superior bandwidth efficiency. For telemetry links that are power-limited, however, some of the bandwidth efficiency obtained by using SOQPSK can be exchanged for superior detection efficiency. This paper describes one scheme for doing so, trading a 56% increase in bandwidth for a 10 dB improvement in link margin.

2. PRIOR RESULTS

The two fundamental components of the proposed scheme are SOQPSK modulation, and LDPC error correction, so we will start with a brief review of the prior work upon which the present paper is based.

2.1 SOQPSK

SOQPSK is a form of continuous phase modulation (CPM), described in [1] and subsequently defined in IRIG 106 as the Advanced Range Telemetry (ARTM) Tier I waveform, using the values $\rho = 0.70$, $B = 1.25$, $T_1 = 1.5$, and $T2 = 0.50$. With these four specific parameters, the waveform is known as ARTM Tier I or SOQPSK-TG, where the "TG" stands for Telemetry Group.

It is important to note that SOQPSK is a constant envelope modulation, so the linearity of the power amplifier in the transmitter is unimportant. This makes the waveform ideal for use in applications that require compact, high efficiency transmitters.

The shaping applied to the phase trajectory of the underlying Offset QPSK (OQPSK) signal results in a substantial bandwidth reduction from OQPSK, as shown in Figure 1 and Figure 2.

Unfiltered (or unshaped) OQPSK is rarely used for telemetry, due to its poor bandwidth utilization. A more relevant basis of comparison is the legacy PCM/FM modulation used for telemetry since the 1960s. The often-cited bandwidth ratio of 2-to-1, comparing PCM/FM (also referred to as ARTM Tier 0) to SOQPSK, is based on the 99.9% power bandwidth as shown in Figure 2.

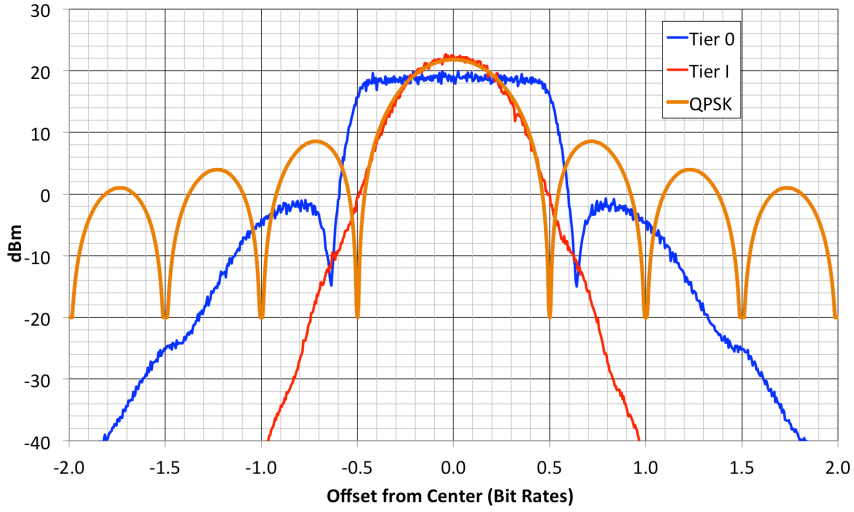

Figure 1: PSD of SOQPSK (Tier I), QPSK and PCM/FM (Tier 0)

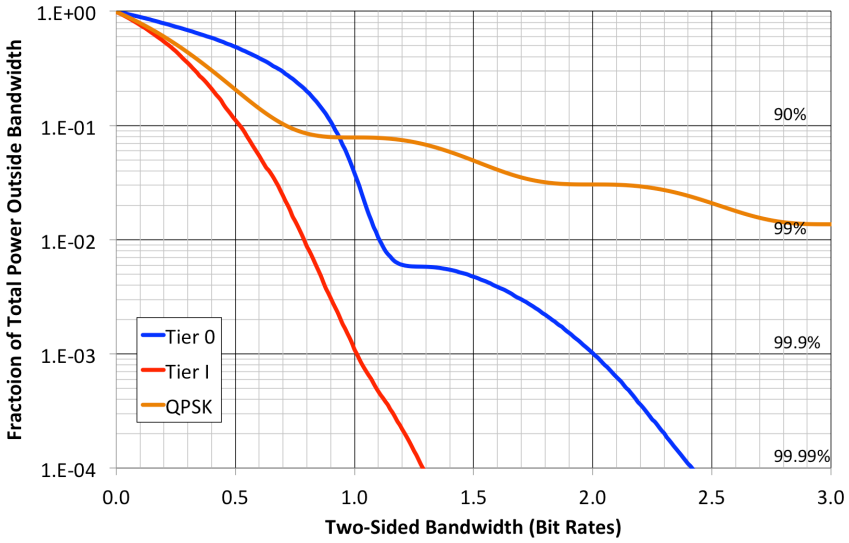

Figure 2: Fractional out-of-band power of SOQPSK, QPSK and PCM/FM

At the time of its introduction, SOQPSK not only occupied half the bandwidth of legacy PCM/FM, but its bit error rate (BER) performance was about 0.7 dB better as well. Later, the introduction of trellis demodulators improved the detection of PCM/FM about 3.5 dB over the best single-symbol PCM/FM demodulators. Therefore, uncoded SOQPSK today operates at about a 2.8 dB disadvantage to the best PCM/FM trellis demodulators. See Figure 3.

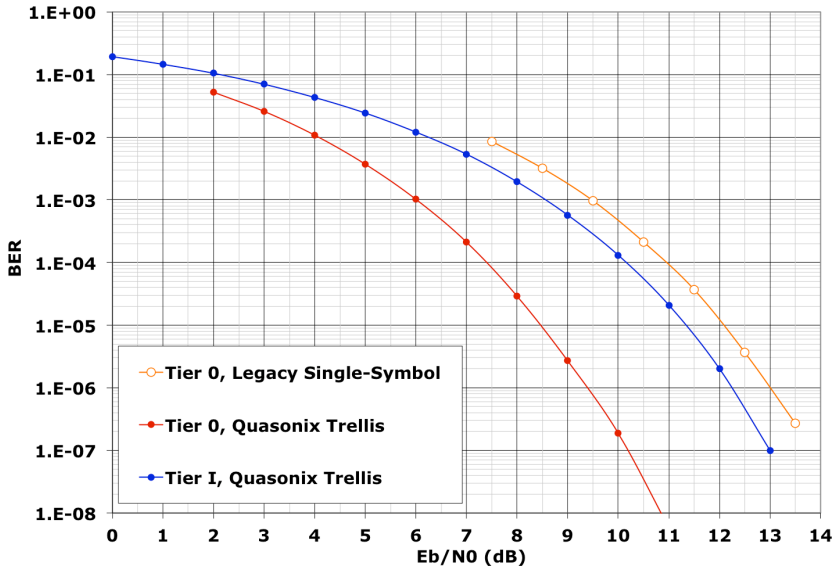

Figure 3: BER of SOQPSK and PCM/FM with both single-symbol and trellis demodulators

2.2 Low Density Parity Check (LDPC) Codes

The LDPC codes are linear block codes, first developed by Robert G. Gallager at M.I.T. in 1960, and published by the M.I.T Press as a monograph in 1963 [2]. Because of their high computational complexity, there were no practical implementations at that time.

The LDPC codes were re-discovered by David J.C. MacKay in 1996 [3], and with the availability of large Field Programmable Gate Arrays (FPGAs), compact implementations became possible. For a given bandwidth expansion, the LDPC codes provide more coding gain than previous codes. For this reason, LDPC codes began displacing turbo codes in the late 1990s, and are now widely deployed in applications demanding high performance:

- 2003: DVB-S2 standard for the satellite digital TV
- 2006: 10GBase-T Ethernet (10 Gbps over twisted-pair)
- 2007: CCSDS as an “Orange Book”
- 2008: ITU-T G.hn standard
- 2009: Wi-Fi 802.11 High Throughput PHY
- 2012: integrated Network Enhanced Telemetry (iNET)

3. PROPOSED SOQPSK/LDPC SCHEME

3.1 Encoder

The Consultative Committee for Space Data Systems (CCSDS) has published an "Orange Book" [4] defining nine different LDPC codes of various code rates and block sizes, as tabulated below.

Information block length k	Code block length n		
	rate 1/2	rate 2/3	rate 4/5
1024	2048	1536	1280
4096	8192	6144	5120
16384	32768	24576	20480

The integrated Network Enhanced Telemetry (iNET) standard specifies the rate 2/3 (6144, 4096) code, and we propose to utilize this same code in the present work. The encoder for this code is depicted in Figure 4, where M = 1024, m = 256, and K = 4.

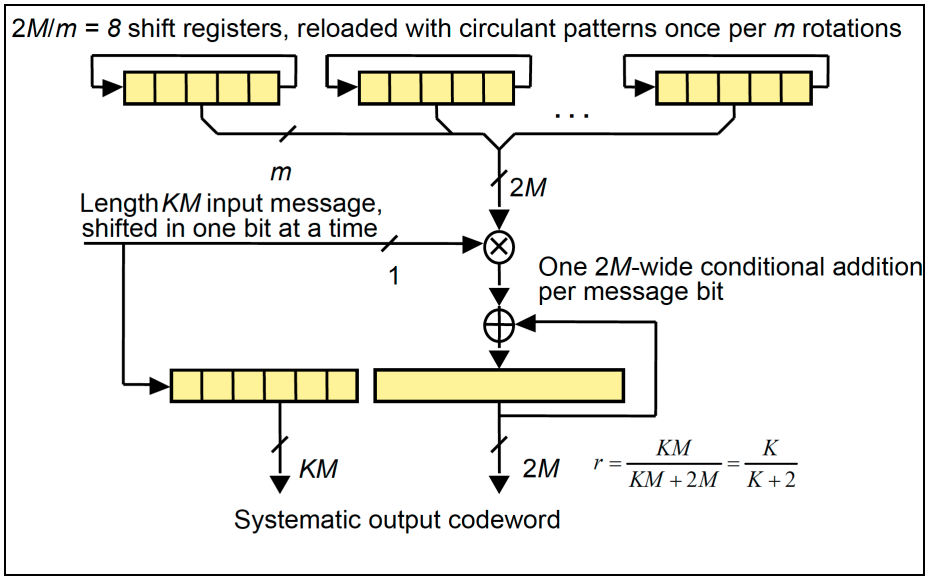

Figure 4: Encoder for proposed LDPC code

3.2 Synchronization

Since the LDPC codes are block codes, the decoder must know where the code word starts. In order to provide this information reliably, even at very low Eb/N0, it is necessary to include known synchronization words in the transmitted signal. This is accomplished by prepending a 256-bit synchronization word to every LDPC code word. The steps in assembling a transmit packet are as follows:

1. Input 4096 data bits (randomize prior to encoding, if necessary)
2. Compute and append 2048 parity bits
3. Prepend 256-bit attached sync marker (ASM). The ASM is constructed as A, A, Ā, A, where

   A = FCB88938D8D76A4F (hex)

   Ā = 034776C7272895B0 (hex)

The completed packet, comprising 6400 bits, is shown in Figure 5. The packet is transmitted leftmost bits first. The first few bits are 1111110010111000...

Figure 5: Packet assembly

Building the ASM from 64-bit sub-words allows for future applications where the four 64-bit sub-words can be used as a heavily coded four-bit preamble (to select other codes, for example).

The synchronizer for the proposed scheme is implemented as a 256-bit hard-decision correlator, with a correlation threshold of 192. As shown in Figure 6, a correlation threshold of 192 yields reliable LDPC word sync at least 3 to 4 dB below the code's useful threshold, and provides a negligible false alarm rate.

It is important to note that the proposed packet structure contains all the information necessary for code word synchronization with each and every code word. The inclusion of the ASM with every code word yields a fresh opportunity to synchronize every 4096 payload data bits, with only 4% overhead.

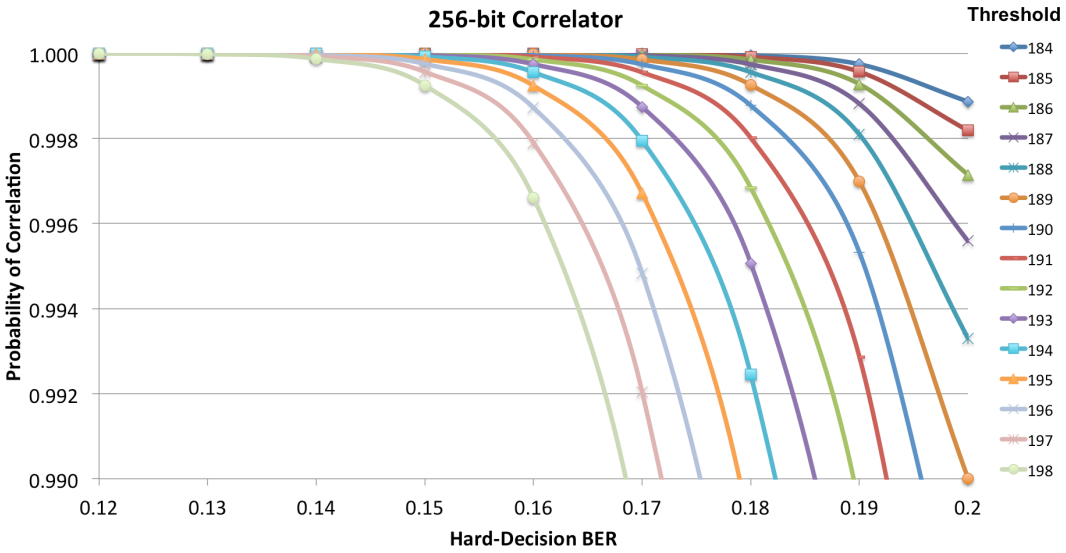

Figure 6: Probability of Detecting Initial ASM

The effectiveness of this synchronization scheme is demonstrated in Figure 7, which shows the receiver IF output at three values of Eb/N0: +35 dB, +3 dB, and -6 dB. Even at -6 dB, the correlator provides consistent synchronization pulses.

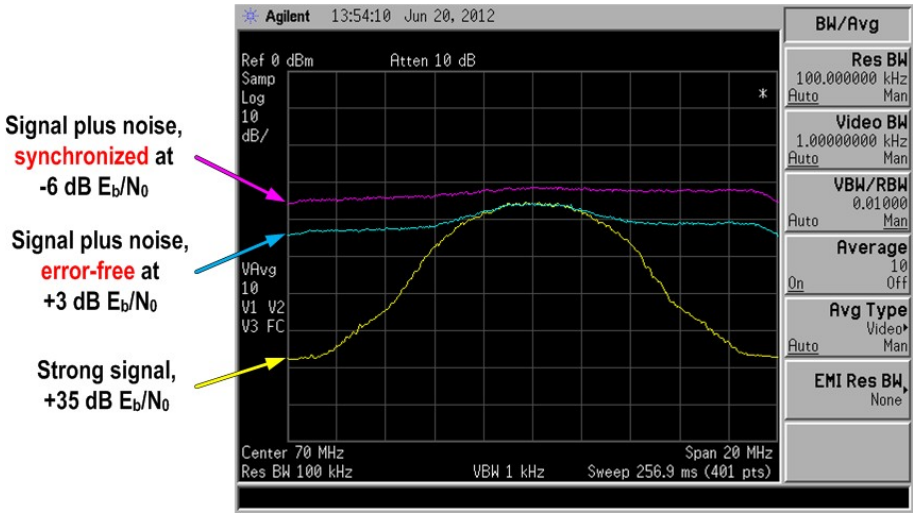

Figure 7: Receiver IF Output During 7 Mb/s LDPC Operation

Once the receiver has synchronized to a single ASM, it continues to develop a stronger correlation estimate by averaging correlations over a small sliding window. This further extends the range below the code's useful threshold, below which block synchronization can be maintained, without significantly extending the time required to detect loss of sync. In the present implementation, the ASM averaging window is 4 code blocks, which yields the approximate probability of maintaining block synchronization shown in Figure 8.

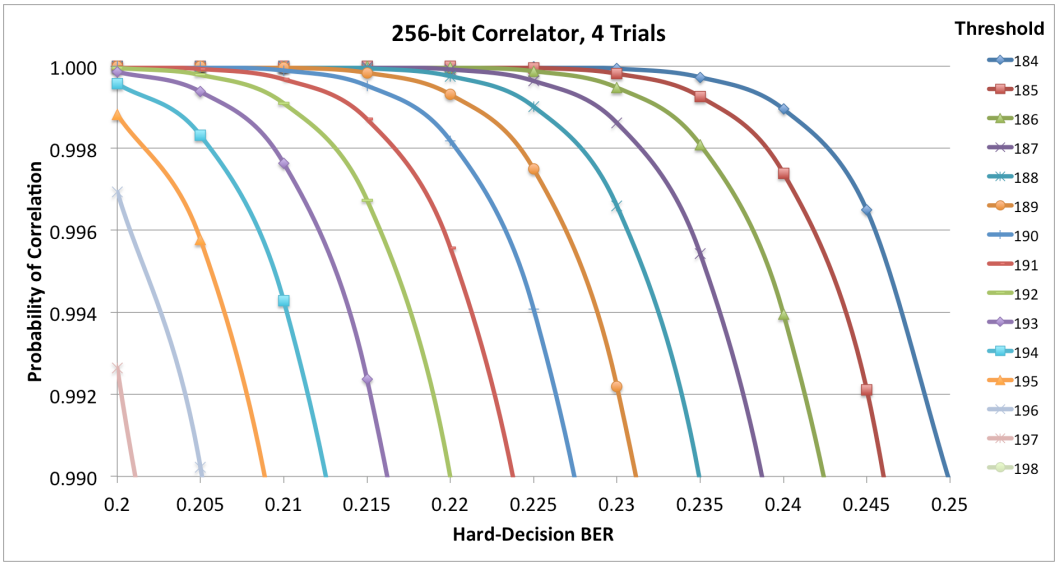

Figure 8: Probability of Maintaining Block Sync, 4 Block Average

3.3 Decoding

Decoding the LDPC code word requires demodulating the SOQPSK waveform with soft decisions. Iterative decoders generally work best with high-resolution soft decisions, so the system was built and tested using 8-bit soft decisions. The decoder also requires an estimate of the Eb/N0 for soft decision scaling.

While the decoder uses soft decisions, the ASM correlator uses hard decisions. Its purpose is two-fold: to identify the start of the LDPC code word, and to resolve the 4-ary phase ambiguity in SOQPSK.

In the proposed scheme, there are no gaps in the transmitted signal, so the decoder can only execute decode iterations until next code word arrives. For this reason, the coding gain varies with bit rate, as shown later.

4. IMPLEMENTATION

4.1 Encoder

The encoder is implemented in an Altera Cyclone III FPGA. It utilizes approximately 4800 logic cells and 3 M9K RAM blocks, which includes all the resources necessary to perform data buffering, ASM insertion, encoding, and 25/16ths input-to-output rate synthesis. The encoder is capable of running at a rate exceeding the transmitter's output bandwidth, that is, in excess of 80 Mb/s.

4.2 Decoder

The decoder is implemented in an Altera Stratix IV FPGA. It utilizes approximately 33,000 ALUTs, 125 M9K RAM blocks, and 1 M144K RAM block, which includes all the resources necessary to perform soft decision scaling, data buffering, ASM detection and removal, decoding, and 16/25ths input-to-output rate synthesis. The decoder is capable of running at the receiver's maximum bit rate of 46 Mb/s. However, the number of decoding iterations scales inversely (and automatically) with bit rate, such that only about 30 iterations can generally be attempted at the highest bit rate.

5. LABORATORY PERFORMANCE RESULTS

5.1 Spectral Characterization

The 2048 parity bits and 256 bits of ASM result in a transmitted packet of 6400 bits, which carries 4096 payload data bits. This results in a bandwidth expansion of 6400/4096, or 25/16. Measured results for the power spectral density and fractional out-of-band power are shown in Figure 9 and Figure 10, respectively.

Referring to the 99.9% bandwidth in Figure 10, it's easy to see that the bandwidth expansion of 25/16 is exactly as expected. It is also worth noting that this bandwidth is still 22% less bandwidth than the legacy PCM/FM waveform at the same payload data rate.

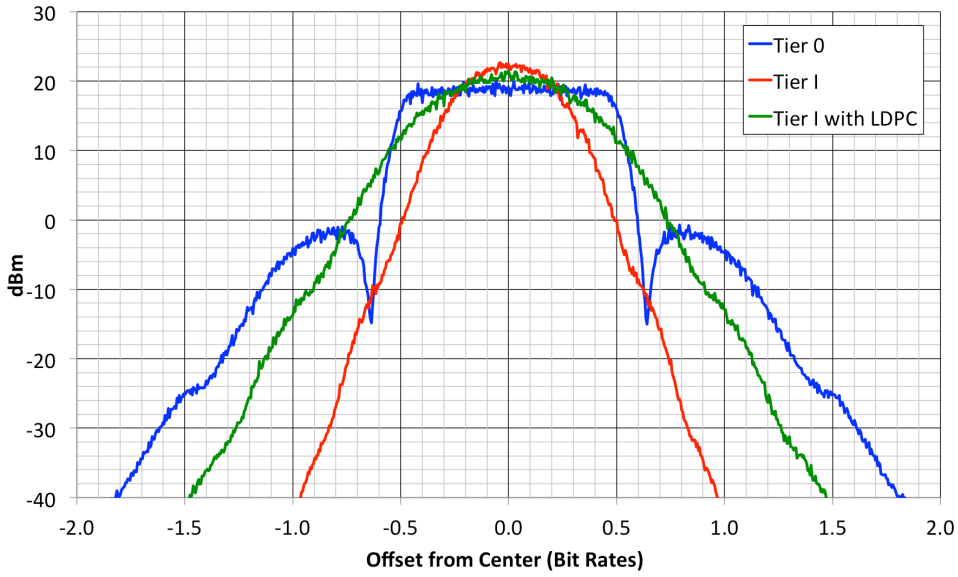

Figure 9: Power spectral density, with coding

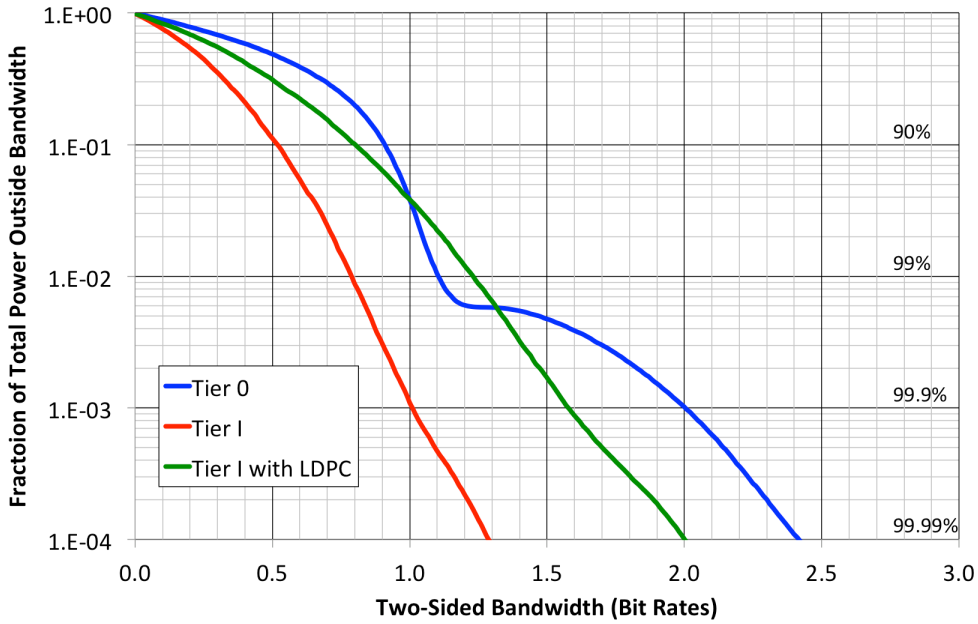

Figure 10: Fractional out-of-band power, with coding

5.2 Bit Error Rate Performance

The whole point of adding forward error correction to any communications system is to operate at lower Eb/N0. The proposed SOQPSK/LDPC readily achieves this objective, offering a coding gain of approximately 10 dB at BER = 10^{-6}, as shown in Figure 11. The actual coding gain depends on the number of iterations the decoder can complete in the available time, so the coding gain is somewhat higher at lower bit rates.

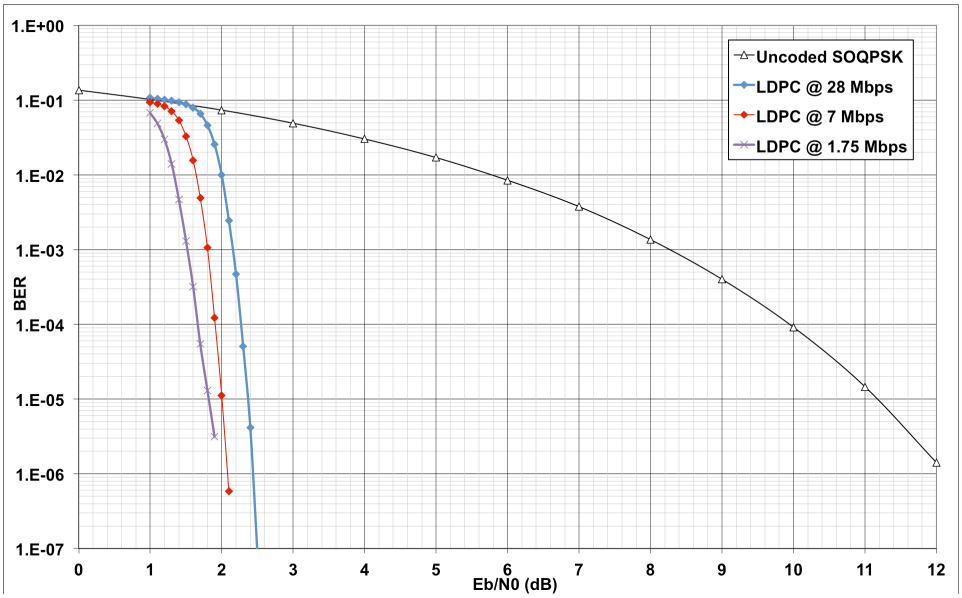

Figure 11: Measured bit error rate performance

The proposed decoder was implemented in an Altera Stratix IV FPGA, where the decoder could run 200 iterations at a 7 Mbps payload data rate. As shown in Figure 12, comparison of the measured BER results for this case (solid red curve) with previously published results (solid blue curve) for this same code at 200 iterations, shows virtually perfect agreement with previous results.

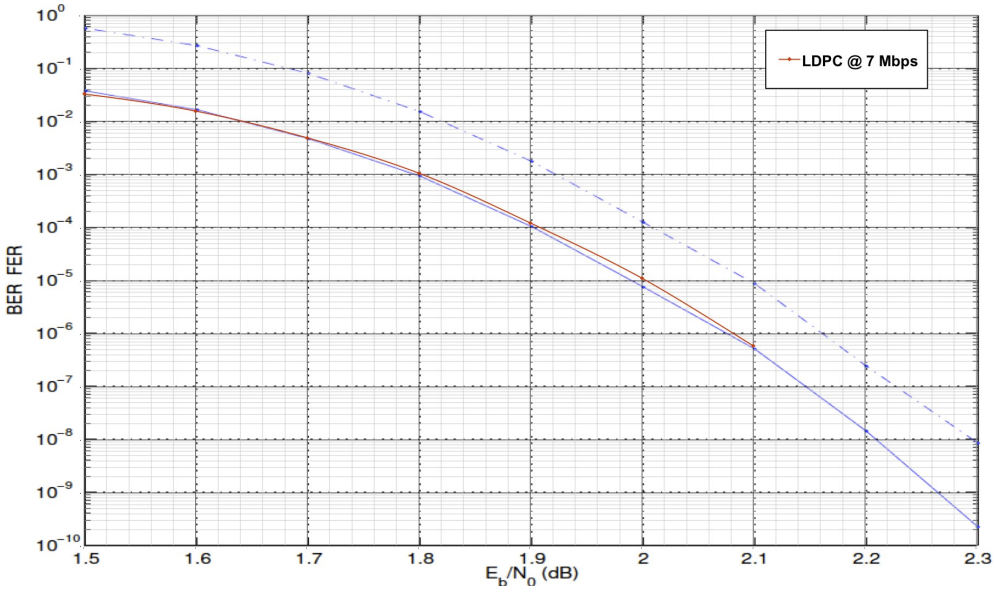

Figure 12: Measured BER performance (red curve), compared with previous results (solid blue curve)

5.1 ASM Detection Results

The effectiveness of the sliding window average for ASM synchronization was verified by setting the input signal 3 dB below the 10^{-5} BER threshold level, measuring raw error rate at the

input to the ASM detector (approximately 15%), and then measuring the duty cycle of the ASM detect signal. This measurement was performed using an oscilloscope that accumulates statistics across multiple untriggered sweeps, and taking the duty cycle as $(V_{avg} - V_{det}) / (V_{loss} - V_{det})$, where V_{avg} is the average voltage, V_{det} is the voltage when ASM is detected (approximately 0 VDC), and V_{loss} is the voltage when ASM is lost (approximately 5 VDC).

In order to generate measurable drop rates, the ASM detect threshold had to be artificially raised. Values used were 208, 210, 212, and 214. With these thresholds, the following results were recorded:

Threshold	Expected Duty Cycle	Measured Duty Cycle
208	0.09%	0.19%
210	0.69%	0.85%
212	3.65%	3.40%
214	13.21%	10.10%

These results confirm that ASM synchronization is maintained under conditions of extremely high BEP, as long as the demodulator can maintain carrier phase and bit timing synchronization.

Achieving carrier phase and bit timing lock at the low E_b/N_0 supported by this LDPC code is not a trivial task for the demodulator, and we have only preliminary results in this area. Two different demodulators were evaluated for the SOQPSK / LDPC configuration, and the synchronization performance of those two demodulators will be the subject of a separate publication. Suffice it to say that the results presented here are based on a fully coherent SOQPSK demodulator, which exhibits highly variable carrier phase synchronization times, particularly at low E_b/N_0. Preliminary results with a "limited coherence" demodulator show much faster carrier phase acquisition (on the order of 2 to 3 LDPC code blocks), but this demodulator exhibits a significant phase slip rate at low SNR, which the present decoder does not tolerate. Further research is under way in this area.

6. FIELD PERFORMANCE RESULTS

The system described in this paper has been delivered to multiple DoD test ranges, and the field measurements have demonstrated that the predicted link margin improvement is indeed realized in the field. Additional tests are underway at both Edwards AFB and Eglin AFB, and results will be reported when they become available.

7. CONCLUSIONS

The bandwidth efficiency versus detection efficiency of the proposed SOQPSK/LDPC scheme is shown in Figure 13, along with several other modulations of interest to the telemetry community. All the modulations shown are constant envelope modulations, which maintain their performance even when amplified with nonlinear amplifiers.

PCM/FM with single-symbol detection has been the standard scheme in aeronautical telemetry since the 1960s, and many flight test programs continue to use it even today. The proposed SOQPSK/LDPC scheme uses 22% less bandwidth than this legacy approach (measured at the 99.9% bandwidth), while providing approximately 10 dB more link margin.

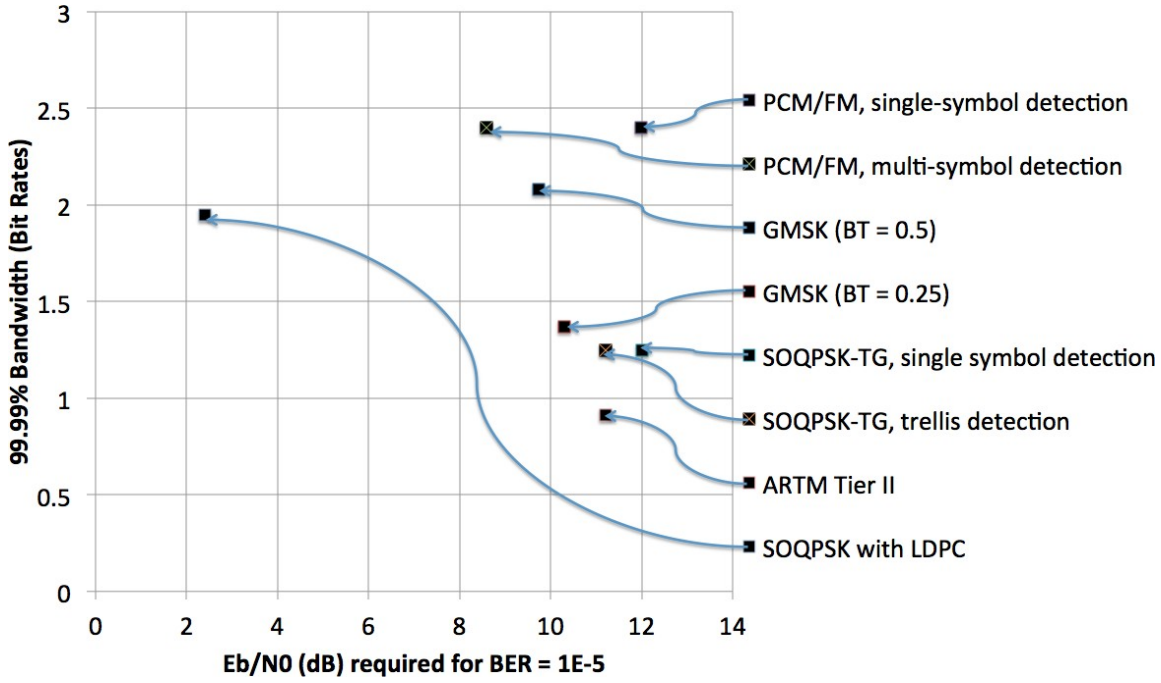

Figure 13: Bandwidth and detection efficiency of several constant-envelope modulations

Summarizing the key points of this paper, we have shown the following:

- The proposed rate 2/3 LDPC code with SOQPSK yields approximately 10 dB of coding gain at BER = 10^{-6}, relative to uncoded SOQPSK.
- Coding gain varies approximately ±0.5 dB, depending on data rate.
- Coding gain is maintained, even when the signal is amplified with nonlinear amplifiers, because the SOQPSK modulation is constant envelope.
- The 256-bit ASM provides reliable, fast code block synchronization at E_b/N_0 below the code's useful operating threshold.
- With a fully coherent SOQPSK demodulator, carrier phase synchronization proves to be the limiting factor in initial acquisition. Further research is required in this area.
- The bandwidth expansion of the proposed scheme is 25/16, which is still 22% less bandwidth than legacy PCM/FM at the same payload data rate.
- Implementation complexity is reasonable for today's FPGAs.
- For power-limited channels, SOQPSK with LDPC offers an attractive trade of spectral efficiency for a significant gain in detection efficiency.

8. REFERENCES

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